CLAIMS

What is claimed is:

1. A system for providing substantially matched bias signals, comprising:

a signal compensator that provides a compensation signal that combines with one of first and second bias signals to mitigate a difference between the first and second bias signals, the signal compensator provides the compensation signal based on third and fourth signal generated to emulate the first and second bias signals, respectively.

2. The system of claim 1, further comprising a compensation buffer that provides a control signal based on a difference between the third and fourth signals, the signal compensator provides the compensation signal based on the control signal.

3. The system of claim 2, further comprising:

a first current source coupled to provide the third signal to emulate the first bias signal; and

a second current source coupled to provide the fourth signal to emulate the second bias signal,

the third and fourth signals being provided to an input of the compensation buffer, the compensation buffer provides the control signal based on a difference between the third and fourth signals.

4. The system of claim 2, further comprising a voltage supply that provides a reference voltage to the compensation buffer, the reference voltage being near a midpoint of high and low voltage rails implemented by the system.

5. The system of claim 4, the voltage supply further comprising a voltage divider coupled between the voltage rails.

6. The system of claim 1, further comprising at least one current mirror coupled to supply the compensation signal to the one of the first and second bias signals based on the control signal.

7. The system of claim 6, further comprising:

a first current mirror coupled to supply a first compensation signal to the first bias signal based on the third and fourth signals; and

a second current mirror coupled to supply a second compensation signal to the second bias signal based on the third and fourth signals.

8. An amplifier comprising the system of claim 1.

9. The amplifier of claim 8 further comprising an input buffer that is biased by the first and second bias signals, the amplifier provides an output based on an input signal provided to an input of the input buffer.

10. The amplifier of claim 10, the input buffer further comprising a pair of diodes coupled in series between respective inputs to which the first and second bias signals are provided, the input of the input buffer defines a node between the pair of diodes, the input corresponds to one of an inverting and a non-inverting input of the input buffer.

11. An amplifier system comprising:

an input buffer having at least one input that receives an input signal, the input buffer is biased by respective signals received at first and second bias inputs thereof; and

a signal compensator that provides a compensation signal to at least one of the first and second bias inputs so that the respective signals received by the input buffer at the first and second bias inputs substantially match each other, the compensation corresponds to a difference between first and second bias signals.

12. The amplifier of claim 11, further comprising:

a first current source that provides a first bias signal to the first bias input;

a second current source that provides a second bias signal to the second bias input;

a third current source that provides a third current to emulate the first bias signal; and

a fourth current source that provides a fourth current to emulate the second bias signal,

the signal compensator provides the compensation signal based on the third and fourth signals.

13. The amplifier of claim 12, further comprising a compensation buffer that provides a control signal based on a difference between the third and fourth signals, the signal compensator provides the compensation signal based on the control signal.

14. The amplifier of claim 13, further comprising a voltage supply that supplies a reference voltage to the compensation buffer, the reference voltage being near a midpoint of high and low voltage rails implemented by the system.

15. The amplifier of claim 14, the voltage supply further comprising a voltage divider coupled between the voltage rails.

16. The amplifier of claim 13, the signal compensator further comprising at least one current mirror coupled to supply the compensation signal to the one of the first and second bias inputs based on the control signal.

17. The amplifier of claim 16, further comprising:

a first current mirror coupled to supply a first compensation signal to the first bias input based on the third and fourth signals; and

a second current mirror coupled to supply a second compensation signal to the second bias input based on the third and fourth signals.

18. The amplifier of claim 11, further comprising an output stage coupled to the input buffer, the output stage providing an output signal based on the input signal provided at the at least one input of the input buffer.

19. An integrated circuit comprising the amplifier of claim 11.

20. A system for providing substantially matched bias signals, comprising:

means for emulating first and second bias signals that are provided to bias an associated circuit; and

means for providing a compensation signal that combines with at least one of first and second bias signals to mitigate a difference between the first and second bias signals, the compensation signal being provided based on third and fourth signals provided by the means for emulating.

21. The system of claim 20, further comprising means for providing a difference signal based on a difference between the third and fourth signals provided by the means for emulating, the means for providing further providing the compensation signal based on the difference signal.

22. The system of claim 21, further comprising:

means for supplying a first compensation signal to the first bias signal based on the difference signal; and

means for supplying a second compensation signal to the second bias signal based on the difference signal.

23. An amplifier comprising the system of claim 20, the amplifier further comprising means for buffering an amplifier input signal, the means for buffering being biased based on the first and second bias signals and the compensation signal, whereby mismatch in biasing the means for buffering is mitigated.

24. A method for improving bias matching of an amplifier, comprising:

providing first and second bias signals at first and second bias inputs of an amplifier;

generating third and fourth signals to emulate the first and second bias signals; and

providing a compensation signal to at least one of the first and second bias inputs based on the third and fourth signals, such that aggregate signals at each of the first and second bias inputs substantially match.

25. The method of claim 24, the providing the compensation signal further comprising:

supplying a first compensation signal to the first bias signal based on a difference between the third and fourth signals; and

supplying a second compensation signal to the second bias signal based on the difference between the third and fourth signals.

26. The method of claim 25, further comprising controlling which of the first and second compensation signals is provided based on a characteristic associated with the difference between the third and fourth signals.